IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): R.A. Corley et al.
Case: 1-1
Serial No.: 10/630,961
Filing Date: July 30, 2003
Group: 2416
Examiner: Mon Cheri S. Davenport

Title: Processor Configured for Efficient Processing of Single-Cell Protocol Data Units

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APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants (hereinafter "Appellants") appeal the rejection dated November 25, 2008, of claims 1-14 of the above-identified application. A Notice of Appeal is submitted herewith.

The fee previously paid with the prior Notice of Appeal filed January 17, 2008 should be applied to the present Notice of Appeal, and the fee previously paid with the prior Appeal Brief filed March 17, 2008 should be applied to the present Appeal Brief. Please charge the difference between the current fees and the amounts previously paid to Deposit Account No. 50-0762.

Appellants note that this is the third appeal brief filed in the present application. It is believed that the failure of the Examiner to permit the present application to proceed to the Board is resulting in an inefficient use of resources for Appellants and the U.S. Patent and Trademark Office, as well as an inordinate delay in prosecution. Accordingly, the present application should be permitted to proceed to the Board for a decision on the merits.

REAL PARTY IN INTEREST

The present application is assigned of record to Agere Systems Inc. On April 2, 2007, the assignee Agere Systems Inc. completed a merger with LSI Logic Corporation, with the resulting entity being named LSI Corporation. LSI Corporation is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals or interferences.

STATUS OF CLAIMS

The present application was filed on July 30, 2003 with claims 1-14, all of which remain pending. Claims 1, 13 and 14 are the independent claims.

Each of claims 1-14 stands rejected under 35 U.S.C. §103(a). Claims 1-14 are appealed.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a processor comprising controller circuitry and first memory circuitry internal to the processor. The controller circuitry is configurable to determine for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit. The processor is connectable to a second memory circuitry external to the processor. Information characterizing the given protocol data unit is stored in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit, and information characterizing the given protocol data unit is stored in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

Illustrative embodiments of the processor recited in claim 1 are described in the specification at, for example, page 5, lines 1-19, with reference to FIG. 1. A processor (e.g., network processor 102) comprises controller circuitry (e.g., controller 120) and first memory circuitry (e.g., internal memory 104) internal to the processor. The controller circuitry is

configurable to determine for a given protocol data unit received by the processor (e.g., from network 108) whether the given protocol data unit is a single-cell protocol data unit (see, e.g., page 5, lines 17-19, of the specification). The processor is connectable to a second memory circuitry (e.g., external memory 106) external to the processor. Information characterizing the given protocol data unit is stored in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit (e.g., single-cell storage portion 122, described at page 5, lines 13-15, of the specification), and information characterizing the given protocol data unit is stored in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit (e.g., multi-cell linked list storage portion 124, described at page 5, lines 15-17, of the specification).

Independent claim 13 is directed to a method for use in a processor comprising controller circuitry and first memory circuitry internal to the processor. The processor is connectable to second memory circuitry external to the processor. The method comprises the steps of determining for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit; storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit; and storing information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

Illustrative embodiments of the method recited in claim 13 are described in the specification at, for example, page 7, line 6, to page 8, line 8, with reference to FIG. 3. A method (e.g., that shown in flow diagram 300) is suitable for use in a processor (e.g., 102 in FIG. 1) comprising controller circuitry (e.g., controller 120 in FIG. 1) and first memory circuitry (e.g., internal memory 104 in FIG. 1) internal to the processor. The processor is connectable to second memory circuitry (e.g., external memory 106 in FIG. 1) external to the processor. The method comprises the steps of determining for a given protocol data unit received by the processor (e.g., in step 302) whether the given protocol data unit is a single-cell protocol data unit (e.g., step 304); storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit (e.g., step 306); and storing

information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit (e.g., step 308).

Independent claim 14 is directed to a processor-readable medium containing processor-executable instructions for use in a processor comprising controller circuitry and first memory circuitry internal to the processor. The processor is connectable to second memory circuitry external to the processor. The instructions when executed in the processor implement the steps of determining for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit; storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit; and storing information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

Illustrative embodiments of the medium recited in claim 14 are described in the specification at, for example, page 6, lines 7-11, with reference to FIG. 1, and page 7, lines 21-22, with reference to FIG. 3. A processor-readable medium contains processor-executable instructions (e.g., software code, as recited in the specification at, for example, page 6, lines 7-11, with reference to FIG. 1, and page 7, lines 21-22, with reference to FIG. 3) for use in a processor (e.g., 102 in FIG. 1) comprising controller circuitry (e.g., controller 120 in FIG. 1) and first memory circuitry (e.g., internal memory 104 in FIG. 1) internal to the processor. The processor is connectable to second memory circuitry (e.g., external memory 106 in FIG. 1) external to the processor. The instructions when executed in the processor implement the steps of determining for a given protocol data unit received by the processor (e.g., step 302 in FIG. 3) whether the given protocol data unit is a single-cell protocol data unit (e.g., step 304 in FIG. 3); storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit (e.g., step 306 in FIG. 3); and storing information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit (e.g., step 308 in FIG. 3).

The claimed invention provides a number of significant advantages over conventional arrangements. In an illustrative embodiment, single-cell protocol data units are stored in an internal memory of the processor, thereby reducing the number of accesses to external memory.

This results in improved processor performance and throughput. See also the specification at, for example, page 3, lines 9-13, and page 7, lines 6-13.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-14 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,278,834 (hereinafter "Mazzola") in view of V.C. Hamacher et al., *Computer Organization*, 2d ed. 1984, pages 1-9 (hereinafter "Hamacher").

ARGUMENT

Appellants respectfully traverse the §103(a) rejection on the ground that the Mazzola and Hamacher references, even if assumed to be combinable, fail to teach or suggest all the claim limitations, and further that no cogent motivation has been identified for combining the references or for modifying the reference teachings to reach the claimed invention.

In formulating the rejection of claim 1, the Examiner argues, with reference to FIG. 1 of Mazzola, that memory 14a and 14b are the recited first memory circuitry and memory 14c is the recited second memory circuitry. Even if one accepts these characterizations, Appellants respectfully submit that Mazzola still fails to teach or suggest the limitation of claim 1 wherein information characterizing a given protocol data unit is stored in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit, and information characterizing the given protocol data unit is stored in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

Rather than teaching the arrangement recited above, Mazzola instead teaches an arrangement wherein a single-cell protocol data unit is stored within a single memory buffer and a multiple-cell protocol data unit is stored in a linked list comprising multiple buffers. See, e.g., Mazzola at column 4, lines 3-25. However, whether a given protocol data unit is a single-cell protocol data unit stored within a single memory buffer or a multiple-cell protocol data unit stored in a linked list comprising multiple buffers, all memory buffers are allocated within buffer pool 14c (which, as discussed above, the Examiner characterizes as the recited second memory circuitry); see, e.g., Mazzola at column 3, lines 45-47; see also Mazzola at column 4, lines 3-11.

Indeed, the Examiner concedes that buffer pool 14c stores single-cell protocol data units; see the present Office Action at page 3, second and third paragraphs (Memory 14c "is the buffer pool from which memory buffer [sic] are allocated. . . . [T]he buffer contains a protocol data unit big enough to be transmitted as [sic] single data unit.")

In the present Office Action at page 4, first paragraph, the Examiner concedes that Mazzola fails to disclose an arrangement wherein the first memory is internal to the processor. The Examiner relies on lines 3-8 of the second paragraph of page 6 of Hamacher to supplement Mazzola so as to reach the limitations of claim 1.

Appellants respectfully submit that Hamacher contains no teachings or suggestions directed to storage of protocol data units in a memory internal to a processor, or indeed any storage or processing of protocol data units. As such, Appellants submit that nowhere does Hamacher contain any teaching or suggestion which would supplement the conventional arrangement taught by Mazzola so as to reach the limitations of claim 1 wherein information characterizing a given protocol data unit is stored in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit, and information characterizing the given protocol data unit is stored in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

Appellants respectfully submit that, even if the Examiner could somehow establish that all aspects of the invention recited in claim 1 were individually known in the art, such arguments are insufficient to establish a *prima facie* case of obviousness. See, e.g., *KSR International Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (U.S. 2007) ("[A] patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.")

Rather, the Examiner must "identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does." *Id.* (emphasis added) See also *id.* (The analysis of "whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue . . . . should be made explicit.") (emphasis added)

In the present Office Action at page 4, third paragraph, the Examiner asserts that "it would have been obvious to combine Mazzola's invention with Hamacher et al. because internal registers (memory) is 5-10 times faster than external memory to process single-cell PDU's from internal memory. Because doing so would gain a 5-10 times speedup in processing those single-cell PDU's."

Appellants respectfully submit that Mazzola teaches a conventional arrangement similar to that described in the present specification at page 2, lines 1-13, in which a memory external to a processor is used to store all protocol data units, regardless of whether or not such protocol data units are single-cell units.

Appellants respectfully submit that Hamacher's teachings that "[a]ccess times to registers are typically 5 to 10 times faster than memory access times," would not have motivated one skilled in the art to have modified Mazzola so as to store single-cell protocol data units in an internal memory while still storing multiple-cell protocol data units in external memory "[b]ecause doing so would gain a 5-10 times speedup in processing those single-cell PDU's," considering that one could presumably gain a similar "speedup in processing" multiple-cell PDUs by storing all protocol data units in the registers.

Appellants further note that the relied-upon portion of Hamacher states that "not all operands in an ongoing computation reside in the main memory, since processors normally contain a number of high-speed storage elements called *registers*, which may be used for temporary storage of often used operands." (italics in original, underlining supplied)

By contrast, Appellants note that claim 1 is directed to an arrangement wherein information characterizing a given protocol data unit is stored in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit, and information characterizing the given protocol data unit is stored in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit, regardless of the relative frequency with which these protocol data units are used.

Accordingly, Appellants respectfully submit that the Examiner's conclusory assertions that Hamacher would have motivated one having skill in the art to have modified Mazzola so as

to reach the reach the arrangement recited in claim 1 appears to be based on impermissible hindsight, and hence fails to provide a legally sufficient motivation.

Moreover, even if one were to assume for purposes of argument that the Examiner has established a proper *prima facie* case of obviousness, Appellants respectfully submit that there is sufficient evidence of nonobviousness so as to rebut any such *prima facie* case. For example, the fact that others have used a less advantageous technique, rather than combining the teachings disclosed in the cited references, suggests both a long-felt need and failure of others.

Appellants note that Mazzola was filed in 1992 and issued in 1994, and that Hamacher was published in 1984 as the second edition of a book originally published in 1978. Appellants respectfully submit that the failure of other researchers in Appellants' field of endeavor to render the allegedly obvious invention disclosed in the present application, despite the considerable advantages that Appellants have determined result from such an arrangement, during the long period during which both references were publicly available and presumably well known to those skilled in the art constitutes objective evidence of non-obviousness and only further lends support for the patentability of the present invention.

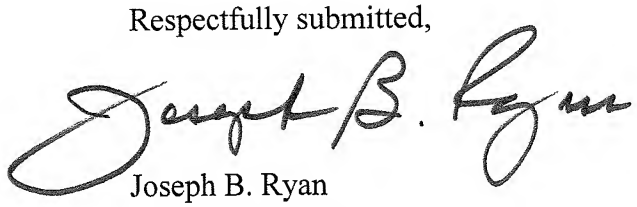
In view of the above, Appellants respectfully submit that the combination of Mazzola and Hamacher fails to render claim 1 obvious.

Independent claims 13 and 14 include limitations similar to those of claim 1, and are believed allowable for reasons similar to those described above with reference to claim 1.

Dependent claims 2-12 are believed allowable for at least the reasons identified above with regard to claim 1.

In view of the above, Appellants believe that claims 1-14 are in condition for allowance, and respectfully request the reversal of the §103(a) rejection.

Respectfully submitted,



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CLAIMS APPENDIX

1. A processor comprising:

controller circuitry configurable to determine for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit; and

first memory circuitry internal to the processor;

the processor being connectable to second memory circuitry external to the processor;

wherein information characterizing the given protocol data unit is stored in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit; and

wherein information characterizing the given protocol data unit is stored in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

2. The processor of claim 1 wherein the protocol data unit comprises a packet.

3. The processor of claim 1 wherein the single-cell protocol data unit comprises a protocol data unit having a size less than or substantially equal to that of a cell-based processing unit of a switch fabric associated with the processor.

4. The processor of claim 1 wherein the information characterizing the given protocol data unit comprises at least one block descriptor.

5. The processor of claim 4 wherein the block descriptor is associated with a particular data block of the given protocol data unit.

6. The processor of claim 1 wherein the information characterizing the given protocol data unit is stored in the first memory circuitry without requiring utilization of a linked list data structure.

7. The processor of claim 1 wherein the information characterizing the given protocol data unit is stored in the second memory circuitry utilizing a linked list data structure.

8. The processor of claim 1 wherein the processor is configured to provide an interface for communication of the protocol data unit between a network and a switch fabric.

9. The processor of claim 1 wherein at least one of the first memory circuitry and the second memory circuitry further comprises a queuing and dispatch buffer memory of the processor.

10. The processor of claim 1 wherein at least one of the first memory circuitry and the second memory circuitry further comprises a protocol data unit buffer memory of the processor.

11. The processor of claim 1 wherein the processor comprises a network processor.

12. The processor of claim 1 wherein the processor is configured as an integrated circuit.

13. A method for use in a processor comprising controller circuitry and first memory circuitry internal to the processor, the processor being connectable to second memory circuitry external to the processor, the method comprising the steps of:

determining for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit;

storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit; and

storing information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

14. A processor-readable medium containing processor-executable instructions for use in a processor comprising controller circuitry and first memory circuitry internal to the processor, the processor being connectable to second memory circuitry external to the processor, the instructions when executed in the processor implementing the steps of:

determining for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit;

storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit; and

storing information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None